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REAL-TIME IMAGING WITH A PULSED COHERENT CO, LASER RADAR

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ABSTRACT

Textron has designed and built under the HI-CLASS (FLD) program a high-powered C02 laser radar for long range targeting and remote sensing. This is a coherent, multi-wavelength system with a two dimensional, wide-band image processing capability. The digital processor produces several output products from the transmitter return signals including range, velocity, angle, and two-dimensional range-Doppler images of hard-body targets. In addition, the processor sorts and reports on data acquired from gaseous targets by wavelength and integrated path absorption. The digital output products are produced in real time and stored off-line for post-mission analysis and further target enhancements. The digital processing algorithms are designed to extract certain features from operation on each of the waveforms. The waveforms are a pulse-tone and a pulse-burst designed for target acquisition and track, and two dimensional imaging (range-Doppler) respectively. The algorithms are categorized by function as acquisition/track, 2D imaging, integrated absorption for gaseous targets, and post mission enhancements such as tomographic reconstructions for multiple looks at targets from different perspectives. Results of the phase 3 field tests (through Feb. 97) will be reported on. The digital imaging system, its architecture, algorithms, simulations, and products will be described. Emphasis of the paper will be to explain the real-time processing architecture and demonstrate the production of real-time, wide-band image products.

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Abstract

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1.0 INTRODUCTION

The HI-CLASS program has been executed in three phases, and at the time of publication of this paper during the first quarter of 97, phase Ill which will produce real-time imaging products at “full” (> 30 joule) transmitted energy levels has just begun. The FLD program will conclude in 1997 with the demonstration of a full-up, real-time operating system. This means the system of transmitter and receiver will operate at 30 Hz (or greater) and all the output products will be computed in real-time and displayed on the operator workstation. The major challenge of the receiver-processor design has been to construct a digital signal processing sub-system which would produce the two dimensional, Fourier Transform intensive, range-Doppler imaging product within 33 msec. and with a minimum latency. The hardware, software and processing architecture which made this possible are the focus of this IRIS paper, with examples of the most recent tracking and imaging products shown. Previous papers on FLD (1, 2, 3) have described other system elements and earlier results, concentrating on such technical issues as the transmitter, heterodyne receiver optical system, analog electronics for signal conditioning and gross Doppler removal, the test program, etc.

The HI-CLASS (FLD) system is currently installed and operating at the Phillips Laboratory AMOS (Air Force Maui Optical Station) observatory on the top of Mt. Haleakala, Maui. The system currently operates in a satellite imaging mode with targets at several hundred Km, and a remote sensing mode where ground targets at 20-40 Km ranges are acquired for identification and analysis. Next generation versions of the laser radar are expected to be airborne with expanded roles in both hard-body (LADAR) and species (LIDAR) targeting.

Table 1 gives a quantitative summary of the HI-CLASS System, with its baseline operating parameters.

Table I HI-CLASS System Characteristics

•Aperture (LBD)	= 0.6M	•Rep Rate	= 30 Hz
•Energy	= 30J	•Wavelength	= 11.15 μ (LADAR) 9-11 μ (LIDAR)
. Transmitter	= Power Oscillator Amplifier	•Waveform	= Pulse Tone (Tracking) Pulse Burst (Imaging)
•Receiver	= Wide-Band (>2 Ghz), Heterodyne Detection, A/D Conversion and Digital Processing		

Figure 1 shows a top-level Conceptual Block Diagram of HI-CLASS. The Receiver-Processor is in effect the controller for FLD with all communication from the Telescope and the entire mount control system going through the Processor. The processor generates the master timing signal and tells the

transmitter when it can fire. Both the laser and the receiving optics are aligned to the Beam Director-Telescope. The processing functions are defined by the particular waveform used: Pulse-tone or Pulse-burst. Figure 2 illustrates the two waveforms, the functional elements of the receiver and processor, and the output. The Pulse-tone waveform is used to acquire the target and to establish the course range and velocity (range rate) estimate. Next in a targeting sequence, the high resolution Pulse-burst waveform is used to produce fine range and velocity measures and to produce range-Doppler and range-amplitude images. HI-CLASS produces a wavefront larger than the target so all "imaging products" are equivalent to ISAR or inverse synthetic aperture radar type images.

See reference 3 for a more detailed explanation of the imaging approach which includes illustrations of output products at intermediate steps of the process.

2.0 RECEIVER-PROCESSOR: ARCHITECTURE AND ALGORITHMS

Figure 3 is a top level block diagram which concentrates on the Receiver and Processor hardware elements and the basic connections. It shows the Processor directing the Transmitter to fire a pulse which goes to and returns from the target through the LBD or Laser Beam Director. Upon return, the optical signal is combined with a signal from the LO to form a heterodyne output which is incident upon a quad (four element) detector. Spurious signal clean-up with an absorption cell and frequency shifting of the return beam using an acousto-optic modulator are performed in the front-end optical heterodyne box as shown. The heterodyned, quad detected signal is passed on to the receiver; and the OPM (Optical Pulse Monitor) signal which comes directly from the transmitter and is combined with the LO beam is sent directly to the digitizer element of the Processor. The RF receiver employs a variable frequency oscillator (VFO) controlled by the Mount Control system estimate through the processor, for target Doppler shift, to provide the Doppler tracking.

2.1 HARDWARE DESCRIPTIONS

Figure 4 shows the receiver and processor in more detail than figure 3 with emphasis on functional descriptions. The receiver functions to amplify detected optical signals, remove gross Doppler frequency shifts under input control by the system processor, amplify the five-channel signals to a level suitable for coherent detection, generate four narrow-band channels for the pulse tone processing and one-wide-band sum signal for pulse burst processing. [t also functions to coherently (with reference to the system 100 MHz clock) replicate the baseband content of the signal generated by the LADAR detector, compensate for Doppler frequency shift, amplify and output to the signal processing at a level suitable for external digital sampling. Prime functions include appropriate controls for frequency offset, gain and bandwidth

of the LADAR receiver detector signal and coherent I&Q LADAR baseband signal output for sampling and processing. The basic operations of summing the four narrow-band signals, normalization, up-conversion-filtering for spur removal and down conversion back to base-band for digitization are illustrated in the figure.

Next, the figure shows the four primary elements of the processor: i.e., the wide and narrow-band A/D's, the core QUAD-C-40/FDAP data processor, the 68040 system controller, and the Sun Spark based operator workstation. The SCRAMNET shared memory-data base structure is a key element for independent development efforts for both software (algorithms) and hardware elements and to adapt the processor for different mission applications.

Figure 5 shows processor hardware elements and is the basis for explanations in further detail of data transfer rates and timing issues associated with the real-time operation of FLD.

Each element operates on the VMEbus standard. One of the VMEbus modules used in the HI-CLASS system is a shared common RAM network card or SCRAMnet. The SCRAMnet network is a replicated shared-memory system (or local area network) implemented over a 150 MBit/See fiber optic ring specifically designed for use in distributed real-time systems. This system allows each device or processing element to transparently share data across the network. The operator work station, data acquisition subsystem, digital signal processor, and transmitter controller are all interconnected via the SCRAMnet network.

2.1.1. Data Acquisition and Control

The data acquisition and control subsystem consists of a VMEbus chassis and a number of COTS modules. The master system and VMEbus controller is an off-the-shelf controller based on the Motorola 68040 processor running the VxWorks real time operating system. Application specific software was written in the C programming language using industry standard development tools. This device provides the basic timing and control for the entire system. Another element of the data acquisition subsystem is an eight channel, 41 MSa/Sec digitizer. This module simultaneously samples both the inphase and quadrature outputs of the quad photomixer that have been converted to baseband for pulse tone processing.

The recording module is based on the Small Computer Systems Interface or SCSI-2. This interface is capable of data transfers at rates up to 20 Mbytes/Sec. The recording medium consists of 4.2 GByte removable hard disk drives. The drives are rated at 14 MByte maximum data transfer rates and can be inserted or removed while the system is powered. There are a total of seven drive slots in the system.

There are a number of miscellaneous components that make up the rest of the data acquisition system including and IRIG decoder for recording system wide time of day, a VMEbus Direct Memory Access (DMA) controller to facilitate data transfers over the VMEbus, and various frequency counters and other sensors for monitoring system status.

2.1.2 Signal Processor

The Signal processor performs all the real time computationally intensive operations. It resides in a separate VMEbus chassis linked to the rest of the system via the SCRAMnet network. Another 68040 based controller resides in this chassis but plays a minor role. There are two independent but identical processing elements consisting of the following.

2.1.2.1 Mizar quad C40 board: The Mizar MZ7772-4 Quad C40 Digital Signal Processing (DSP) engine is a high performance VMEbus processing board with up to four TI (Texas Instruments) TMS320C40 DSPS running at 50 MHz. The TMS320C40 DSP from TI is a floating point processor with six high speed communication ports. The TMS320C40 can process up to 50 million floating point operations per second (MFLOPS) or 25 million integer operations per second (MIOPS).

2.1.2.2 Frequency Domain Array Processor (FDAP): The 66540 Frequency Domain Array Processor from Array Microsystems is a 400 million operations per second VME board that serves as the core of frequency domain operations such as Fast Fourier Transforms (FIT) hand correlations. The FDAP can accept real time data real-time data either from the VMEbus or from external I/0 connectors. The FDAP is rated at 400 million operations per second and the external I/0 interface is rated at 80 Mbytes/sec. The optimized FFT processing engine can calculate a 32K point complex FFT in 6.5 msecs.

A custom interface has been developed to allow data transfers between the external communication ports of the quad C40 board and the external 1/0 interface of the FDAP board supporting the full 80 MByte/see rate of the FDAP.

Although the HI-CLASS system currently uses two of these processing elements, the modular design allows for the insertion of additional processing elements for increased computational power.

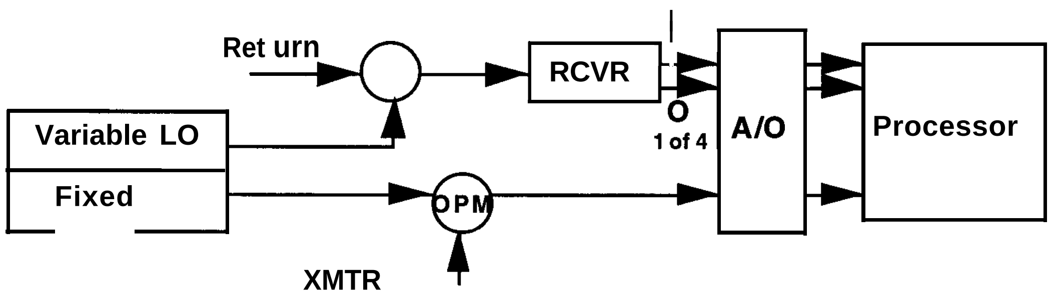
2.2 ACHIEVING REAL-TIME OPERATIONS WITH THE PULSE-TONE WAVEFORM AND ALGORITHM

The previous descriptions of hardware, boards, electronic components with data transfer capabilities and operating speeds, now needs to be complemented with explanations of the software and algorithms which run on

the hardware to show how the system meets the requirements of real-time operation.

The first (in a sequence of operations during a mission) processing executed establishes and maintains track by calculation of the target range and velocity.

The objective of pulse-tone processing is to extract whole body (course) range and Doppler. The method, as illustrated here



is to match-filter the return waveform to the OPM. The following steps make up the complete algorithm:

- Determine PSD of return to find carrier frequency (V_{signal})
- Create "analytic" OPM using Hilbert transform
- FFT OPM
- Generate multiple OPM "filters" shifted to $V_{signal}+k\Delta v$; k=-2 to +2
- Match filter return signal with multiple matched filter returns to extract range and Doppler frequency

Figure 6 shows steps of Matched-Filter processing on the Pulse-Tone waveform. The algorithm/processor produces estimates of both range and Doppler frequency. Figure 6 also shows the calculation steps required to find target azimuth and elevation in order to maintain track. The Az and EL error signals are computed based on sums and differences of incident radiation on the four elements of the QUAD photo detector

In order to acquire and track a target this range-range rate and AzEI offsets must all be computed in real time.

To complete this description of real-time pulse-tone operations an explanation is provided how the algorithm, with its 5 steps listed above, is mapped onto and executed on the core processor. Each step which represents a mathematical operation was benchmarked on the C-40 and FDAP. Figure 7

shows each operation in the algorithm partitioned among the four C-40's and single array processor or FDAP. The net effect is a partially parallel pipeline operation which will execute each frame of data at -33 msec or 30 frames/see with a latency of less than 100 msec.

2.3 REAL-TIME PULSE-BURST PROCESSING AND ALGORITHM ARCHITECTURE

2.3.1 Overview

The pulse-burst waveform is structured to produce high resolution range and cross range information on targets

The pulse-burst algorithm requires two dimensional computation to generate a range and Doppler image and consequently requires more hardware capacity for real-time operation than the pulse-tone process. However, the symmetry of the waveform leads to a relatively simple set of computations, i.e., correlations required to execute the full algorithm. The steps are as follows:

- Segment each return into micropulse intervals
- "Match-filter" micropulse intervals using OPM to remove OPM envelope and modulation
- "Stack micropulse returns ensuring range gates within each micropulse are aligned
- FFT "down" each of the range gates to derive frequency spectrum for each range gate.
- Generate 2-D display

The following detail explains the several processing steps required to prepare the data for and then execute the complete imaging algorithm.

2.3.2. Pulse Burst Processing

2.3.2.1 Data Preparation

Each Pulse Burst waveform is made up of 375 micro-pulses; each micro-pulse is 1.3 nanoseconds in width and the micropulses are spaced 40 nanoseconds apart. The waveforms are sampled at 2 Gsa/sec resulting in eighty range bins per micro-pulse. The return from each micro-pulse is matched filtered with a copy of the out-going micro-pulse (OPM or output pulse monitor) and normalized relative to the output power. Each of eighty range bins is associated with the same range bin for each micro-pulse, forming an 80 column by 375 row array. Each 375 element column is padded to 512 and a Fast Fourier Transform (FFT) is performed. This operation is performed on each

of the 80 columns resulting in an 80 by 512 range Doppler image. The range-amplitude image is formed by averaging the returns in each range bin from all 375 micro-pulses.

The processing is partitioned such that all of the frequency domain processing is performed by the array processor (FDAP). The digitized OPM data and Inphase and Quadrature return signals are transferred to the quad ‘C40 board using the external communication ports. Next, the OPM is transferred to the FDAP and a 32K point real FFT is calculated. The result is transferred back to the quad ‘C40 where the spectrum is unfolded and frequency shifted to baseband, resulting in a complex analytical signal. This is accomplished by re-indexing the FFT frequency bins in the ‘C40. The resulting spectrum is then inverse FFT’d using the FDAP.

2.3.2.2 Matched filtering: As described above, the pulse-burst waveform consists of 375 micro-pulses with 80 range bins per micro-pulse. The 375 points associated with each range bin are extracted and padded to 512 points by the quad ‘C40. Each 512 element array is then FFT’d by the FDAP. This operation is performed on both the OPM and the return waveform. The transform for each micro-pulse of the return waveform is then multiplied by the complex conjugate of the respective OPM transform. Performing the inverse FFT on the result completes the matched filter operation. Each matched filter output is then normalized by dividing by the square of the OPM power.

Range-Doppler image: The quad ‘C40 board forms the 80 by 375 element matrix and pads the 375 element column to 512 element array to the FDAP for FFT processing and then transfers the 80 by 512 range-Doppler image to shared memory for display on the operator workstation. The range-amplitude calculation is straight-forward and is performed by the ‘C40 board.

2.3.2.3 Hardware Architecture: To achieve real-time operations, all the above steps must be executed seamlessly with parallel operations spread over the various components. The key to success was elimination of bottlenecks between the processing engines (FDAP and C-40) by custom design of high-speed interfaces.

Table 2 lists the FDAP requirements and shows the number of bytes of data to be moved through the processor at each step of the labor intensive, frequency domain operations. A pair of FDAPS was selected which could meet these requirements and custom interface boards which could achieve the necessary transfer rates were designed.

Key elements of the interface design are summarized in table 3. Two elements, the FDAP -C-40 interface and the HP scope (wideband A/D) interface were custom designs. The architecture and essential operating parameters which allow full 30 Hz operation are described in tables 4-6.

Summary

These illustrations of the hardware architecture, connections between elements and operational benchmarks of the algorithms in this hardware illustrate the approach taken to achieve real-time operation.

3.0 RESULTS

The brassboard Phase 2 system began operations at AMOS in March of 96’ and has produced significant results. Figure 8 shows processed signals from a satellite target acquired on April 6, 1996, where the range estimates-from HI-CLASS are compared with the traces generated by AIM, and a range plot over 200 seconds of travel is produced. This range plot was significant because we calculated the results in real-time using the on-line processor and also because the span of time covered includes all four Doppler offset positions of the Bragg cell frequency shifter.

Figure 9 shows a major new achievement for phase 2 operations: the acquisition, detection and tracking of uncooperative targets. The raw return, OPM signal and match-filtered output are shown for several representative but large CNR’s. In figure 10 we show the range and velocity products derived from the match-filtering operations.

Next in figure 11 we illustrate range and velocity data calculated using improved, statistical data reduction and analysis techniques. The significance of this figure over the data of April 6 is a significant improvement, approaching the theoretical limit in target range and velocity.

Finally a comparison of figures 12 and 13 show our progress in producing high quality range-Doppler images. In early 1995, using cooperative (LACE and GEOS) targets we demonstrated range-Doppler displays from these retro-reflectors. However, no cross-range Doppler was evident due to the fact that the satellites are stable. To illustrate the full range-Doppler imaging capability of FLD we built a rotating test target and produced two dimensional range-Doppler images at a range of approximately 23 Km. Figure 12 illustrates the early, “Range-no Doppler” returns from two retros on LACE. Figure 13, generated more recently during the last quarter of 96’ shows a complete imaging product of rotating separated retro’s captured at a framing rate of 10 Hz.

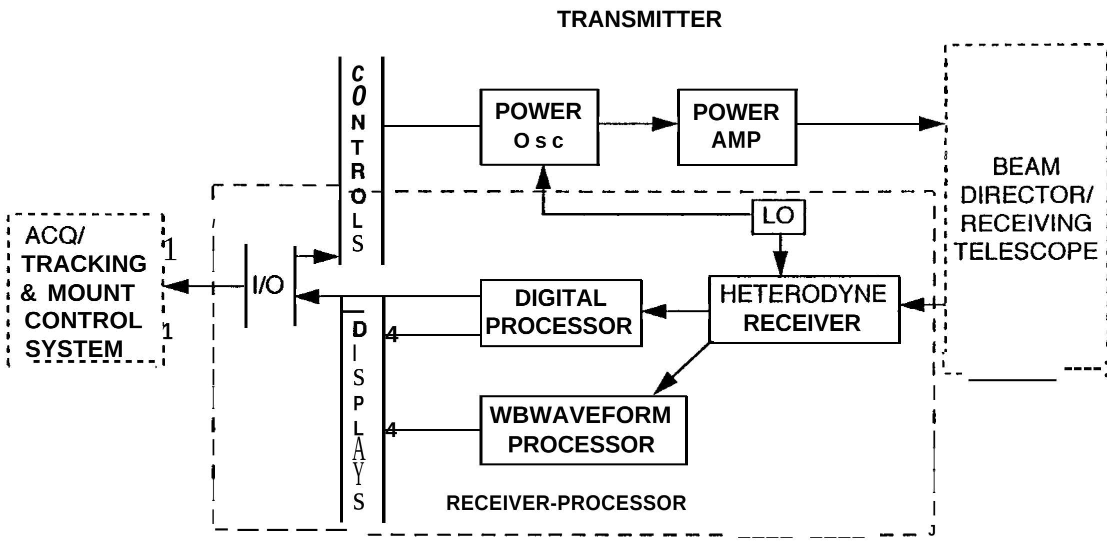
The current stage of our analysis is production of real-time 2D Range-Doppler images using the phase 2 system described in this paper. This work is expected to produce high quality target image products (range-Doppler, integrated and averaged range-amplitude) useful for tracking and classifying hard-body space targets.

4.0 ACKNOWLEDGMENTS

The United States Air Force Phillips Laboratory Laser Imaging Branch has provided management oversight of this effort while the United States Army Space and Strategic Defense Command has monitored the technical effort under contract DASG60-90-C-01 17.

5.0 REFERENCES

1. Design Considerations for a Multi-Channel, Laser Radar Receiver/Processor; Francis Corbett, Gerry Nordstrom, Michael Groden; SPIE, San Jose, Feb., 1996, 2702-12.
2. A Review of the High Class Test Program, Mark Kovacs, Francis Corbett, Subrata Ghoshroy, V. Hasson and Richard Pohle, Textron Systems Division, R. Wendt, USASSDC, Stan Czyzak and Marsha Fox, USAF Phillips Lab., IRIS Active Systems Conference, Eglin AFB, May, 1996.
3. The Digital Image Processor System for a High Powered $C0_2$ Laser Radar, Francis Corbett, Michael Groden, Gordon Dryden, George Pfeiffer, Robert Boos, Textron Systems Division, Douglas Youmans, W.J. Schafer Associates, SPIE, Denver, 1996.



Figurel FLD Conceptual Block Diagram
The Receiver-Processor Elementsareshown inside thedashed lines

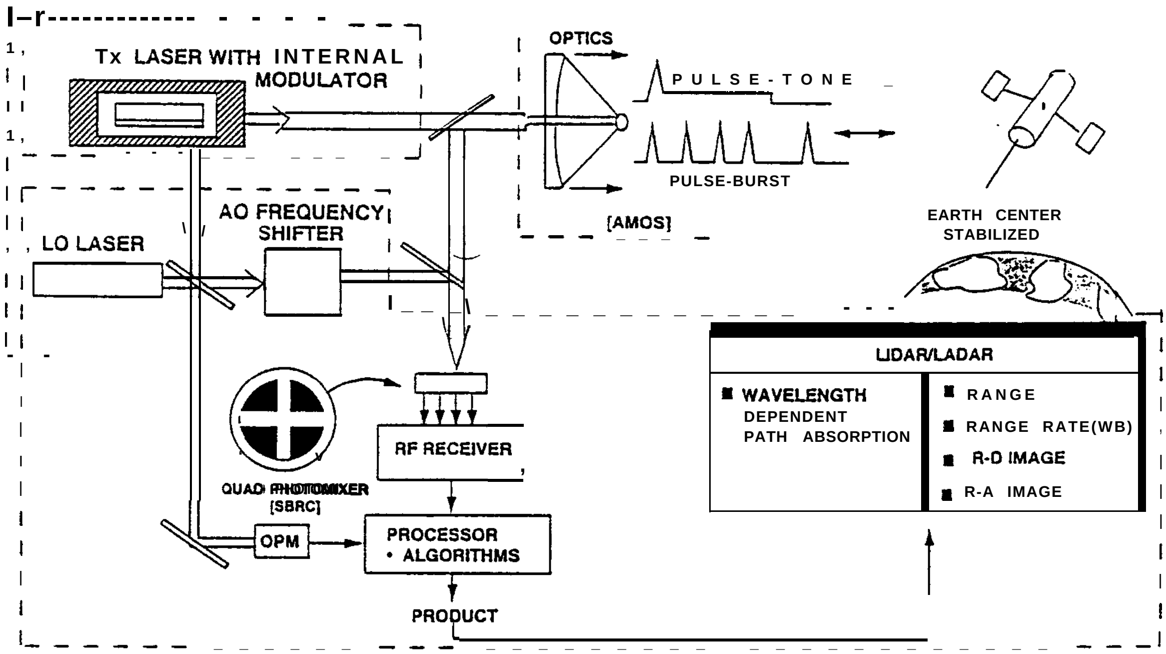


Figure 2 The FLD Data Products Support Both Hard Body and Species Detection
The Pulse-Tone Waveform (see figure) is used to acquire the target, the Pulse-Burst Waveform with <2 nsec subpulses is used to produce fine target detail. Both are employed in analyses of species in the atmosphere.

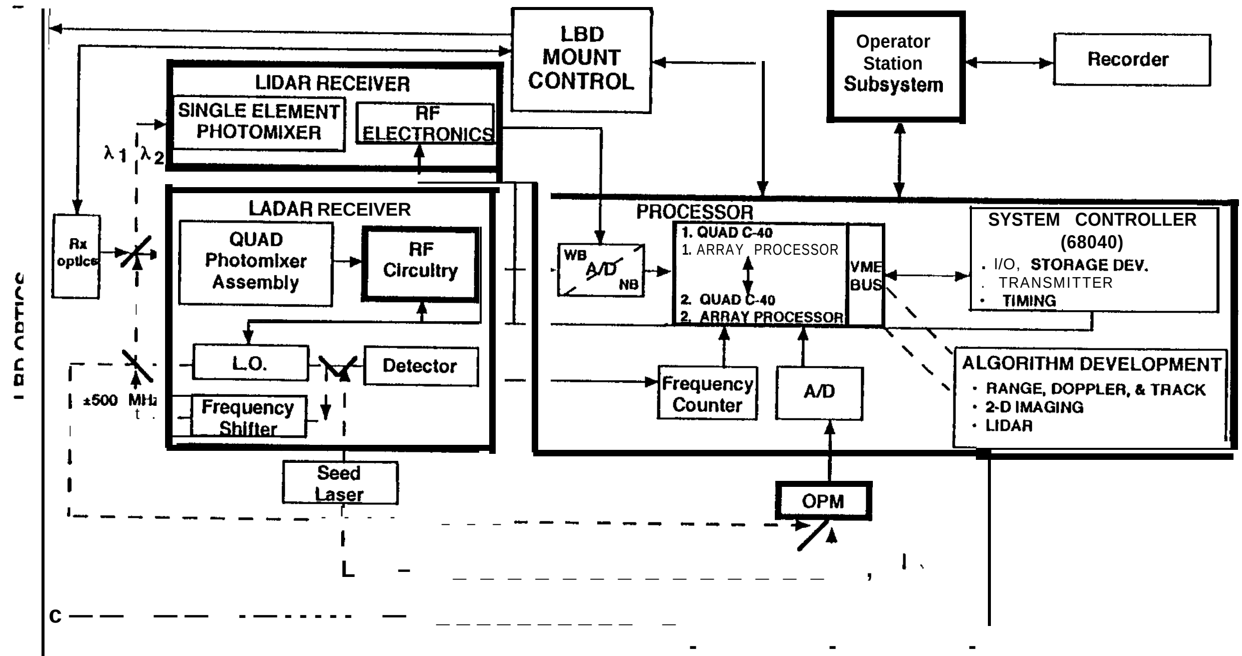


Figure 3 Hi-CLASS Receiver-Processor
Phase 2 Receiver-Processor architecture supports real-timetarget metrics and image generation

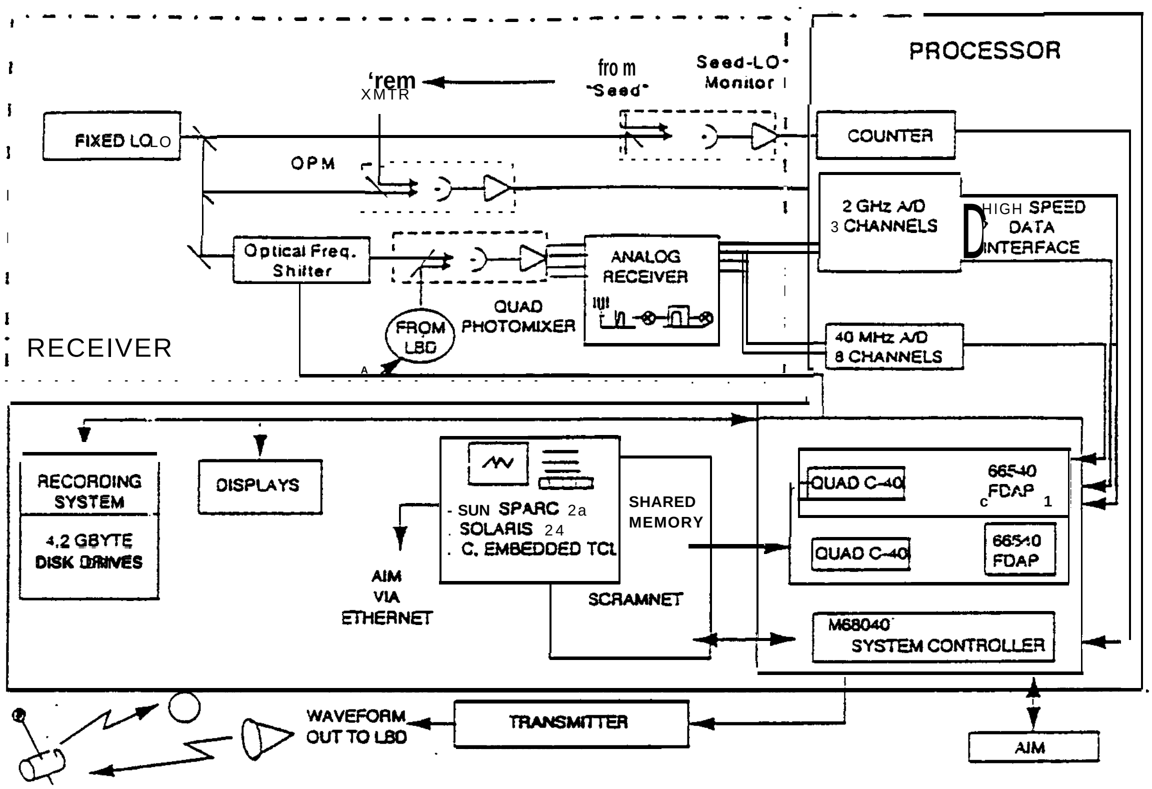
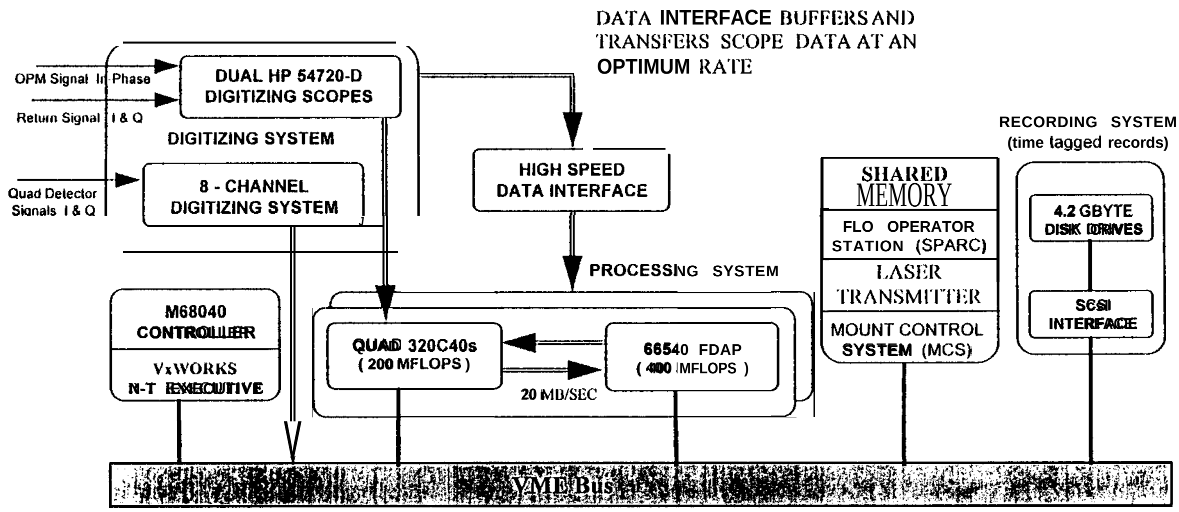


Figure 4 Receiver-Processor Functional Block Diagram
The optical, analog electronics and digital electronic subsystems are shown in further detail



SCRAMNET (SHARED MEMORY NETWORK) ALLOWS EACH SUB-SYSTEM SIMULTANEOUS HIGH SPEED ACCESS TO A COMMON DATA SET

320C40 - ADVANCED DIGITAL SIGNAL PROCESSOR
FDAP - FREQUENCY DOMAIN ARRAY PROCESSOR
M68040 - COTS MOTOROLA M68040 VME COMPUTER BOARD
VXWORKS REAL TIME EXECUTIVE/DEVELOPMENT ENVIRONMENT

Figure 5 Processor Hardware Block Diagram
This VME based system has high speed data interfaces between the A/D and core processor, and within the processor between the C-40 and Array Processors

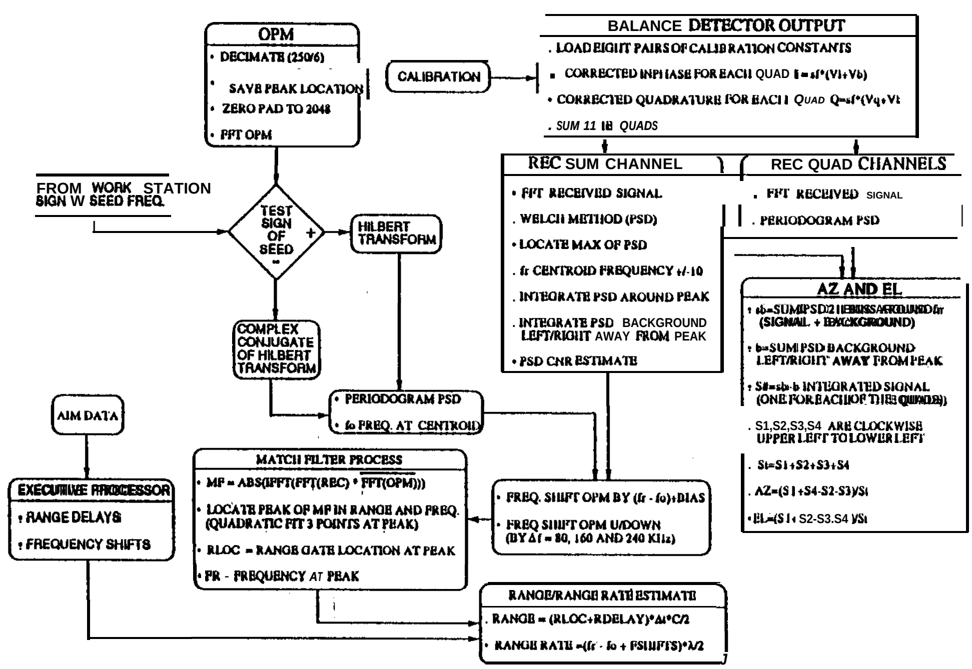


Figure 6 Pulse-Tone Processing Algorithm Flow
Range, velocity, and location (Azimuth and Elevation) are calculated and maintained in real-time

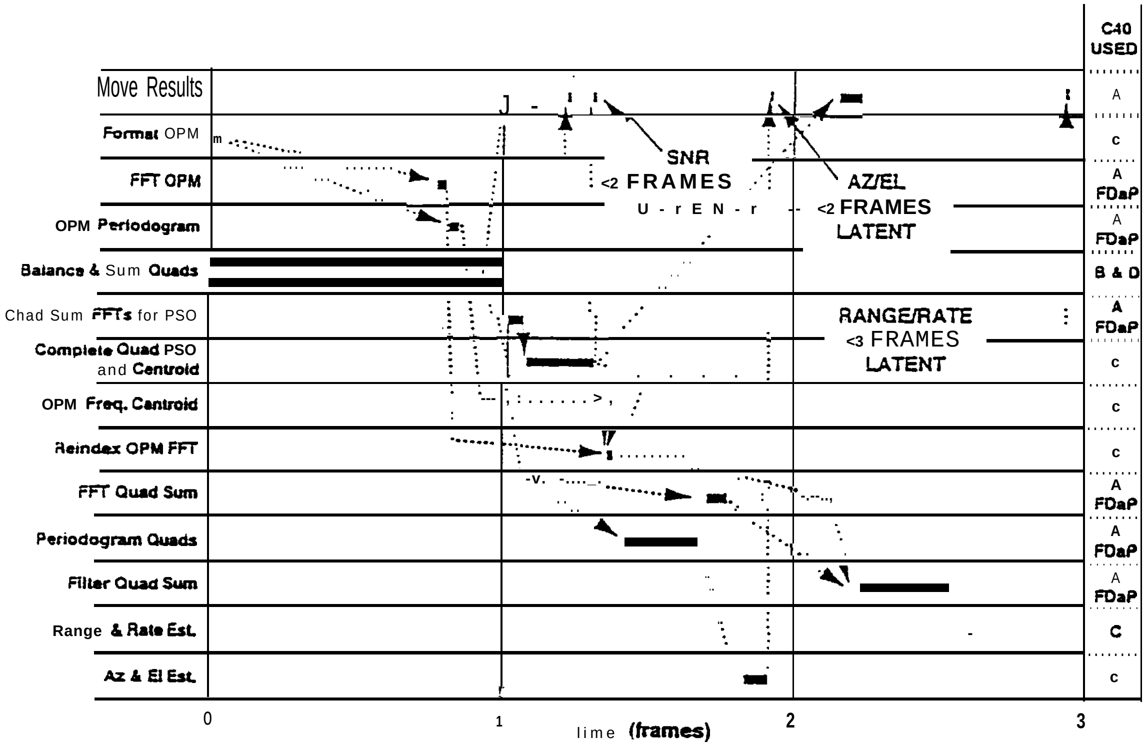
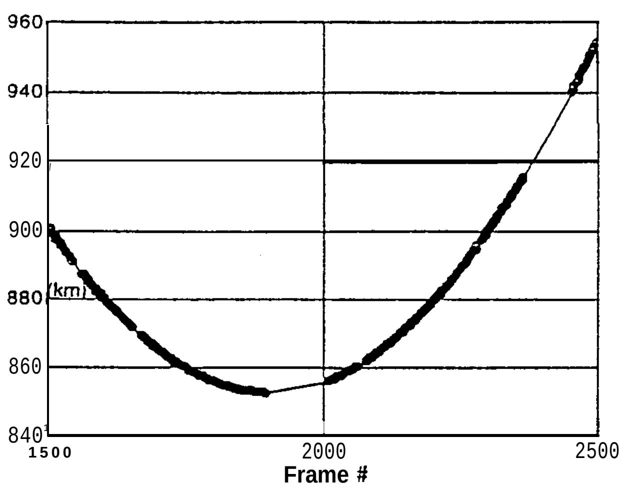


Figure 7 Pulse-Tone Algorithm Mapping onto the

Core QUAD C-40 and Array Processor
Processing times (-33 msec)) and latencies (< 100 msec) are shown

Real-time Derived Range for CNR > 15 dB



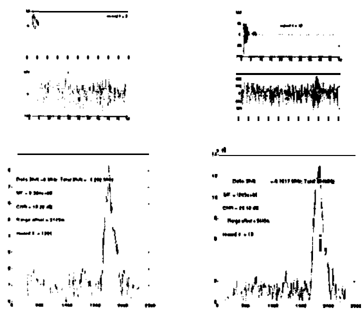
Returns observed for all 4 Doppler offset intervals

Transients at LO frequency changes masked 27 seconds of data returns primarily because frequency changes switched manually.

Figure 8 April 6, GEOS-C Cooperative Target Mission Yielded Return Signals Over a Span > 200 sees

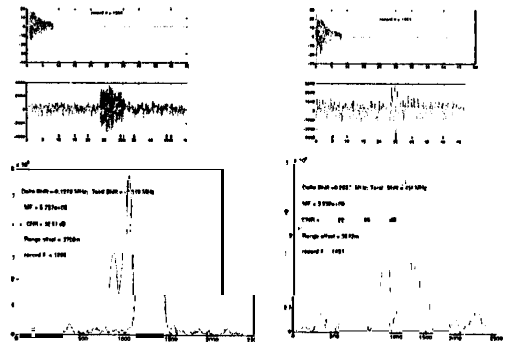
OAO-2 (Obj. 3598) Rocket Body Return (May 9, 1996)

Signals seen over approximately 1.5 second interval with target ε large, implies a very large optical cross section

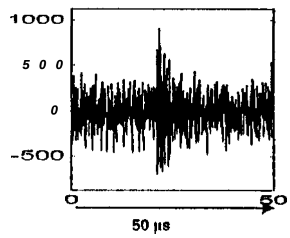


Target @ -14501
Model Prediction
7 Joules, 1 1μs, D= 0.6 m
BQ = 1 , =0.4, QE=0.
CNR = 24 dB with
σ = 100 m²

Tiros-N Return (May 31, 1996) from range= 979 km; Signals detected over 20 second interval

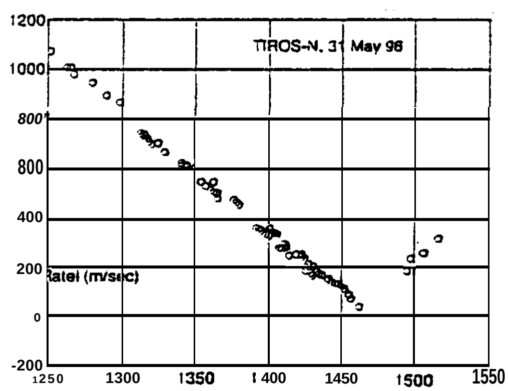


CNR = 32 dB ≥ 150 m²   CNR = 22 dB ≥ 15 m²



Seasat return signal (Nov. 21, 1996) from range (- 900 km) ;
Signals detected over 30 second interval

Figure 9 Strong Return Signals Observed from 3 Uncooperative Satellites



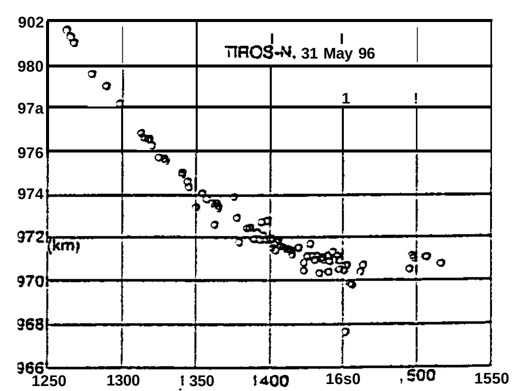


Figure 10 Real-Time Range and Range-Rate are Extracted from Uncooperative Target (Tires-N) Returns

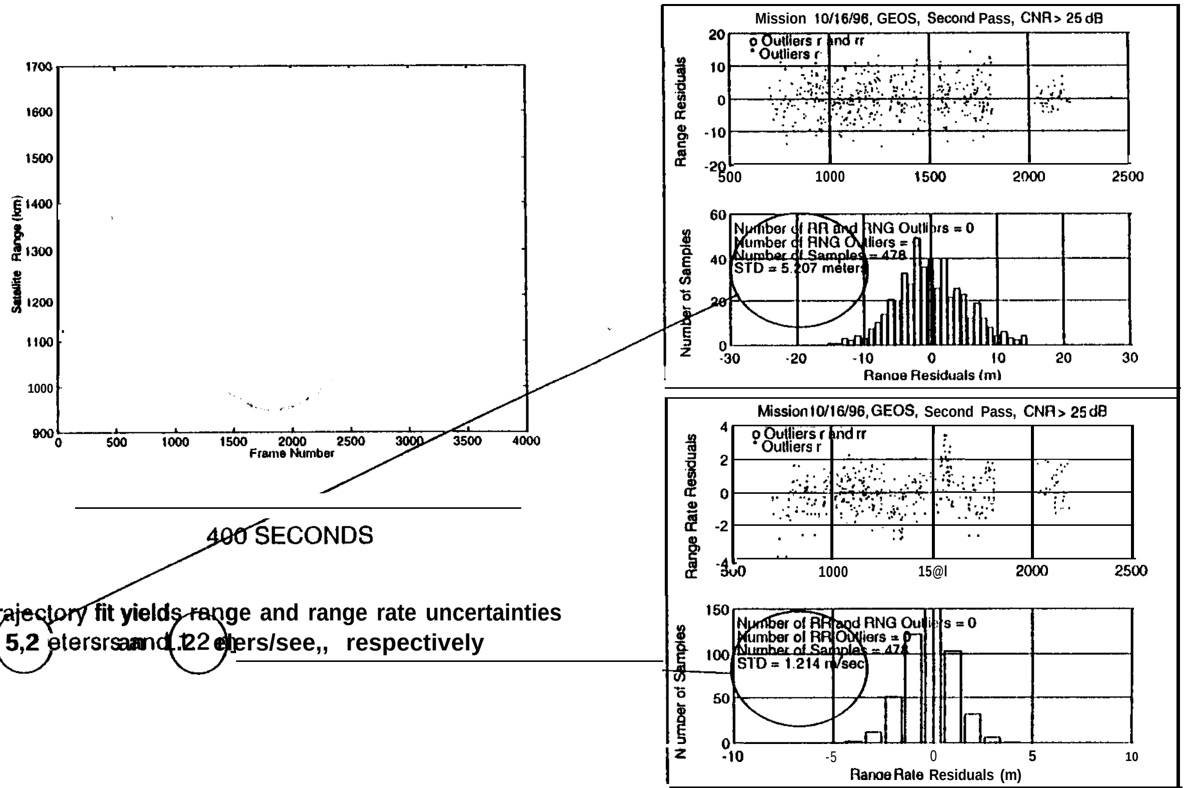
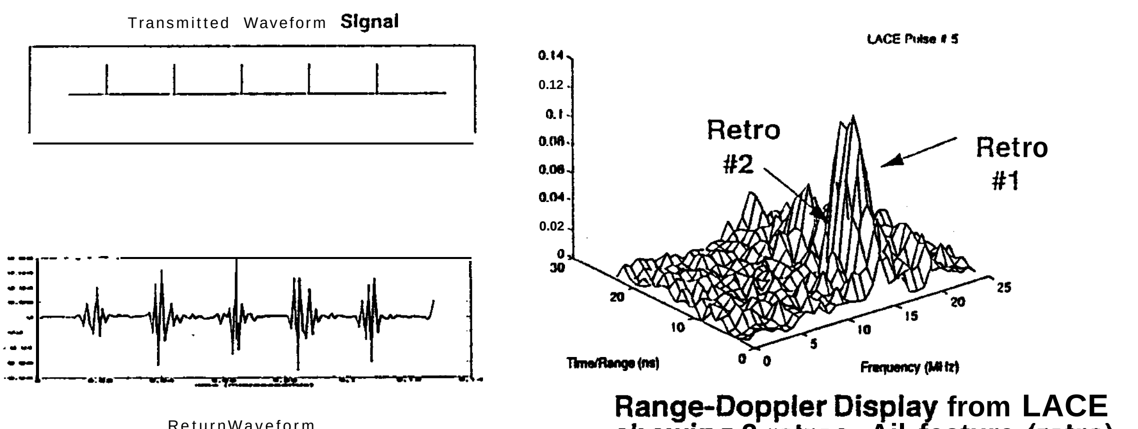
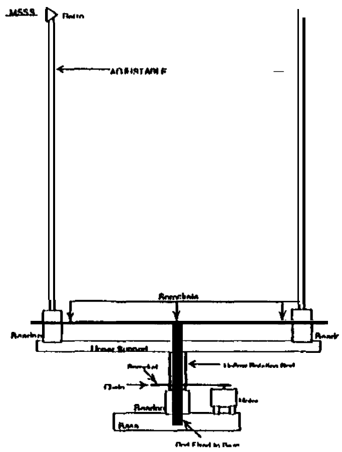


Figure 11 Range Data Generated for Large Portion or 10/16/96 GEOS-C Pass

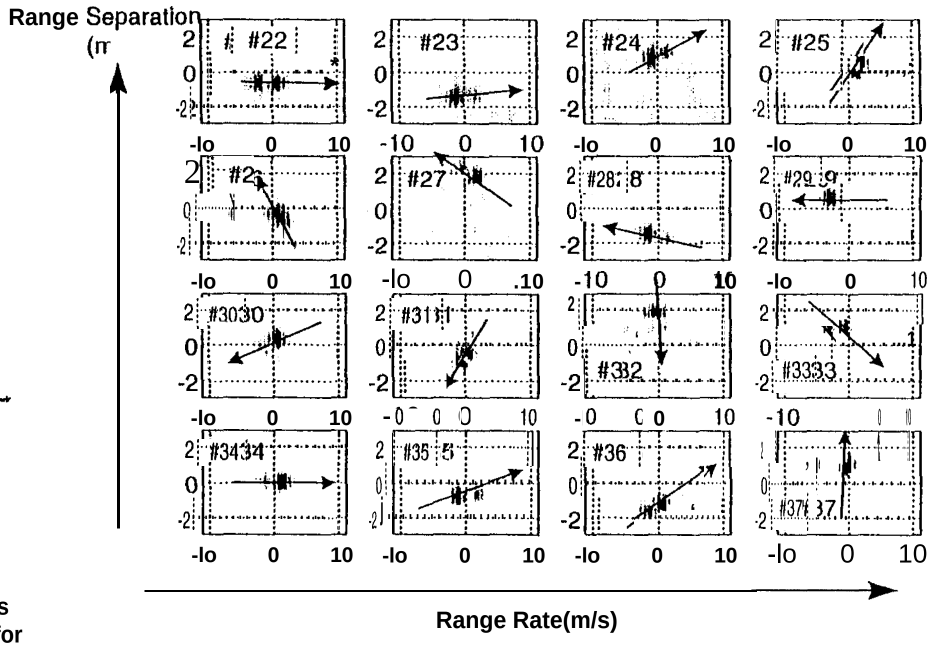


Range-Doppler Display from LACE showing 2 retros. Ail feature (retro) separation is along the range axis. All feature (retro) separation is along the range axis.

Figure 12 Initial Imaging Tests with Cooperative Targets Verified Waveform and Processing Utility



Dual retros separated by 0.5 m and rotating at 0.83 rps (2.6 m/s relative velocity) provide target for imaging demonstration



16 frames captured at 10 Hz show relative range separalion(deiay time) and range rate(Doppler frequency shift) for rotating retros

Figure 13 Dual Rotating Retro-Reflectors Demonstrate FLD Range-Doppler Image Generation Capability

Table 2 Pulse Burst FDAP Processing and i/0 Requirements

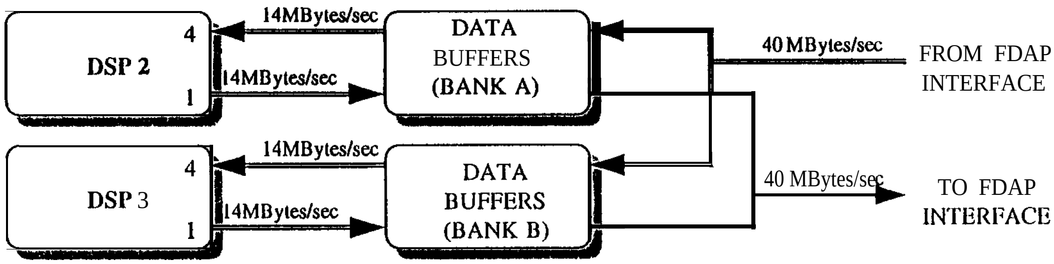
OPERATION	EXECUTION TIME	1/0
FFT OPM	6.561 MSECS.	256K BYTES
IFFT OPM	6.561 MSECS.	256K BYTES
FFT OPM MICRO-PULSES	6.2 MSECS	384K BYTES
FFT RCVD MICRO-PULSES	6.2 MSECS	384K BYTES
IFFT MATCHED FILTERS	6.2 MSECS	384K BYTES
FFT 80 COLUMNS	5.5 MSECS	328K BYES
TOTALS	37.2 MSECS	1992K BYTES

2 MBytes/frame times **15** frames/see implies a 30 MBbytes/sec data rate

Table 3 Custom Interface Design

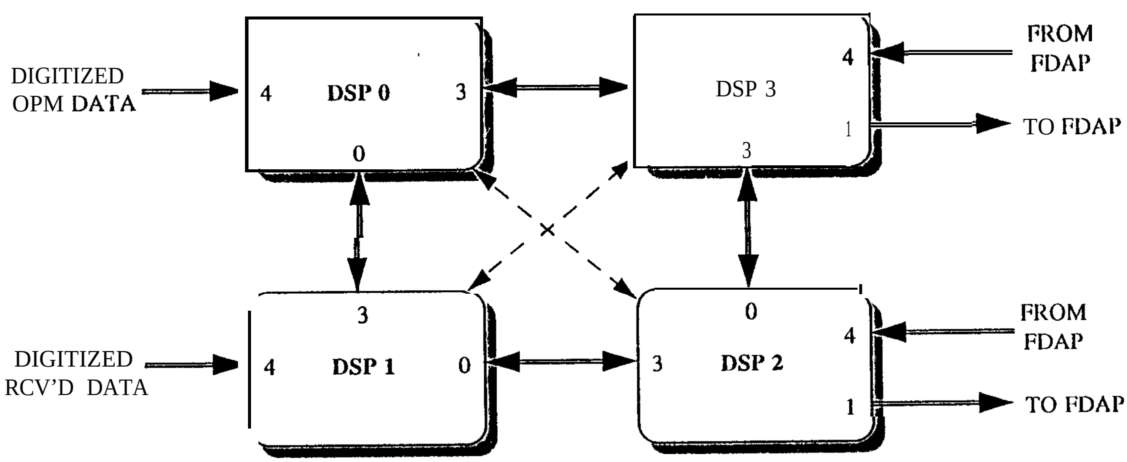
- **Data Transfer Rates**
  - Frequency Domain Array Processor (FDAP) Interface
    - FDAP 1/0 interface can support an 80 MBytes/see data rate.
  - **'C40** Communication Port
    - Comm. ports are rated at 20 MBytes/see
  - Hp scope data Interface
    - One OPM channel and two received signal channels per frame
    - 32K bytes/channel per frame
    - Each HP digitizer can transfer a 16 bit word at a 5 MWord/sec rate. There are two HP digitizers
    - Total data rate 20 mbytes/see maximum
- **Goals**
  - Reduce processor loading and latencies where possible without significant custom hardware design.

Table 4 'C40 to FDAP Interface



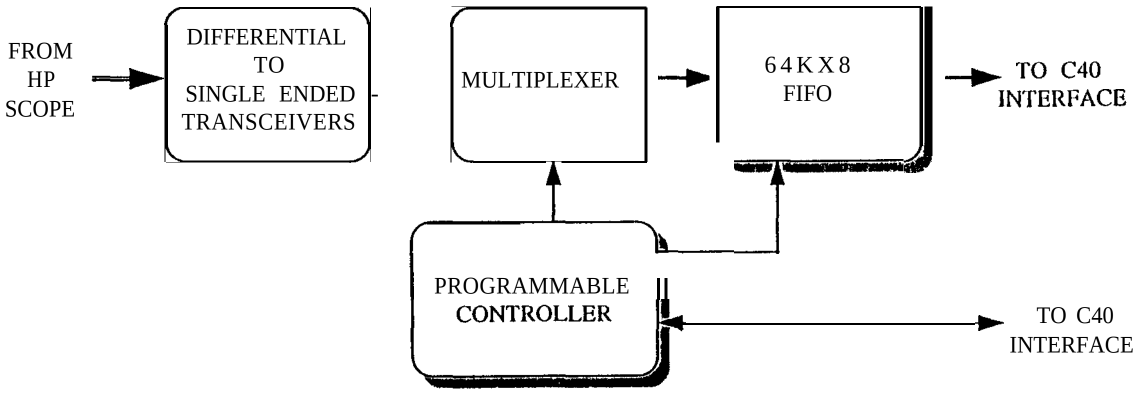
- Two identical data buffers are shared between each 'C40 and the FDAP board
  - Two different DSPS on each 'C40 board can access its FDAP
  - Each 'C40 can transfer data into and out of its data buffer simultaneously
- Data in each comm port channel can be transferred at a 14 MBytes/see rate
- Data can be transferred into and out of the FDAP at an 80 MBytes/see rate
- Interface can be configured **to flush** FDAP processing pipeline without adding overhead to the C40 comm ports

Table 5 'C40 Communication Port Connections



- Comtnunication ports are used for inter-processor communication and external data interfaces.
- Each inter-processor communication port has 20 MBytes/see bandwidth.
- External data interfaces will operate at 14 MBytes/sec .
  - **56** MBytes/see total to FDAP interface
  - 28 MBytes/sec total for HP digitizer intcrface

Table 6 Hp Scope Data Interface



- Hp scope interface can fully buffer one opm frame
- 9 Bits of HP scope data is sign extended **to** 16 **bits**
- OPM data can be interleaved with 16 bits of “zero” data
  - Simulates complex data format
- Signal return channel 1 (inphase) can be interleaved with channel 2 (quadrature)
  - Facilitates processing by the ‘c40 and fdap